Heterogeneous InSb quantum well transistors on silicon for ultra-high speed, low power logic applications

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The heterogeneous integration of InSb quantum well transistors onto silicon substrates is investigated for the first time. 85 nm gate length FETs with $f_T = 305$ GHz at $V_{ds} = 0.5$ V and DC performance suitable for digital logic are demonstrated on material with a buffer just 1.8 μm thick. An initial step towards integrating InSb FETs with mainstream Si CMOS for high-speed, energy-efficient logic applications has been achieved.

Introduction: Indium antimonide has the highest electron mobility and saturation velocity of any known semiconductor, and is therefore a promising candidate for ultra-high speed FETs operating at very low supply voltages. Both enhancement and depletion mode InSb quantum well (QW) transistors with 85 nm physical gate length (L_g) and $f_T > 300$ GHz at $V_{ds} \leq 0.5$ V suitable for direct coupled FET logic (DCFL) have previously been demonstrated [1]. When benchmarked [2] against the state-of-the-art silicon MOSFETs, these devices exhibited more than an order of magnitude improvement in energy-delay product, confirming their potential for ultra-high speed, low power logic applications. However, there remain several significant challenges prior to the implementation of III-V materials for logic [3], one of which is their heterogeneous integration with the Si substrate. A seamless, robust integration would significantly reduce manufacturing costs; the panacea being a blend of low power, high speed III-V digital logic coupled with the functional density advantages provided by the Si CMOS platform.

The InSb QWFET results reported to date were achieved using direct epitaxial growth of InSb quantum-well layers onto (100) semi-insulating GaAs substrates using solid-source molecular beam epitaxy (MBE). In the work reported in this Letter we transferred the InSb quantum-well materials growth onto (100) Si substrates and examined the effect of reducing the thickness of the material present between the Si substrate and the FET channel. The electrical characteristics of the InSb QWs and the RF and DC performance of transistors fabricated from such material are presented.

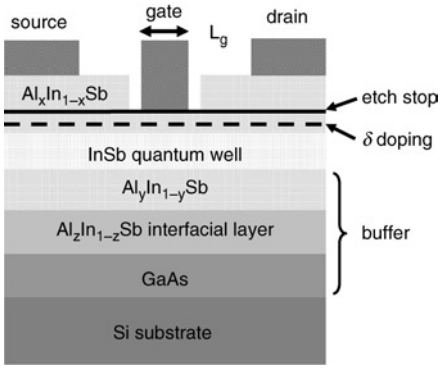

Fig. 1 *Schematic diagram of recessed gate InSb QW transistor*

Materials growth and device fabrication: The active region of the InSb QW well material was grown by MBE onto commercially sourced 4° misoriented (100) GaAs on Si substrates. The complete layer structure from the substrate upward is illustrated in the device schematic of Fig. 1 and consists of a high Al content $Al_zIn_{1-z}Sb$ interfacial layer grown directly onto the GaAs; an $Al_yIn_{1-y}Sb$ ($y = 0.15$) lower barrier layer; a 15 nm InSb QW; a 2 nm-thick $Al_xIn_{1-x}Sb$ ($x = 0.2$) spacer; a Te δ doped donor sheet (1.7×10^{12}cm^{-2}); a 2 nm $Al_xIn_{1-x}Sb$ ($x = 0.2$) spacer; an etch stop and a 26 nm $Al_xIn_{1-x}Sb$ ($x = 0.2$) upper barrier layer. The GaAs, $Al_zIn_{1-z}Sb$ and $Al_yIn_{1-y}Sb$ layers together accommodate the lattice mismatch between the Si substrate and the InSb quantum well and, in this Letter, are collectively termed the buffer. Fig. 2 illustrates the single field Hall data obtained from the material grown on Si. For 6.4 μm-thick buffers, the QW electrical properties are comparable with identical material grown onto GaAs. On reducing the buffer thickness to 1.8 μm the QW conductivity remains high with a carrier mobility of 13800 cm^2/V/s demonstrated at a carrier density of 1.7×10^{12}cm^{-2}.

Recessed gate InSb QW FETs (see Fig. 1) were fabricated from this material. Source and drain ohmic contacts were first defined using optical lithography, then TiAu was deposited by e-beam evaporation. The source-drain separation was 0.75 μm and the contact resistance 0.25 Ω mm. TiAu Schottky gates were then defined using e-beam lithography and recessed down to the etch stop using a highly selective etch chemistry. A wet etch was used to perform mesa isolation and to leave air-bridged gate and drain metal feeds.

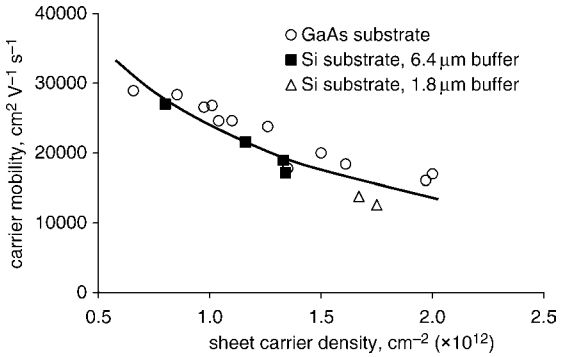

Fig. 2 *Electron mobility against sheet carrier density, from room temperature Hall effect measurements, for InSb QW transistor material grown onto Si or GaAs substrates*

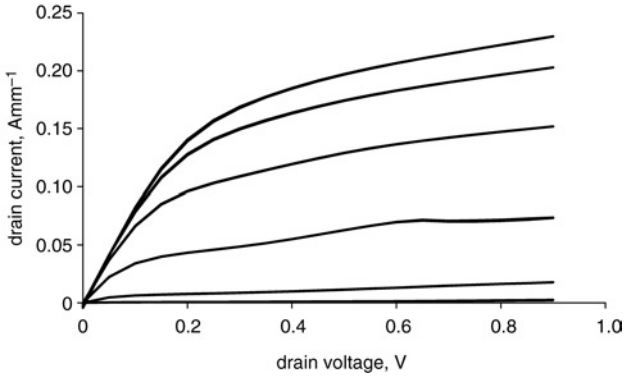

Fig. 3 *Output characteristic for 85 nm L_g InSb QW transistor on 1.8 μm buffer on silicon (gate voltage, V_g, swept from 0.4 to −0.2 V in −0.1 V steps)*

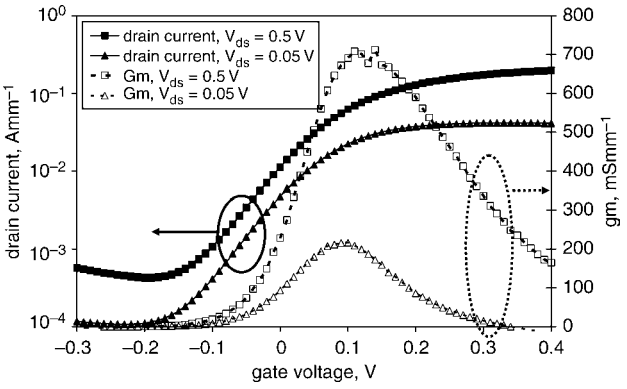

Fig. 4 *Transfer characteristic for 85 nm Lg InSb QW transistor on 1.8 μm buffer on silicon with $V_{ds} = 0.05$ V, and 0.5 V*

Peak transconductance, g_m, for this device was 710 mSmm^{-1} (at $V_G = 110$ mV) and DIBL 82 mV/V

Experimental results and discussion: Typical DC output and transfer characteristics obtained for an 85 nm L_g InSb QW device fabricated from 1.8 μm buffer material on Si are shown in Figs. 3 and 4, respectively. The device is enhancement mode with a threshold voltage, V_T, of +0.01 V and a peak transconductance, g_m, of

710 mS/mm at $V_G = 110$ mV. The 0.5 V gate swing I_{on}/I_{off} ratio, as defined in [2], was 370:1, and, as with previous devices on GaAs substrates, limited by gate leakage. The subthreshold slope was 94 mV/decade making these devices suitable for logic applications. The drain induced barrier lowering (DIBL) was 82 mV/V, confirming scalability and minimal short channel effects. The DC performance of InSb QW FETs on Si demonstrated here equals that achieved in enhancement mode devices on GaAs substrates [1].

To assess RF performance, S-parameter measurements were performed on the devices at frequencies up to 50 GHz using an HP 8510C network analyser. The Si wafer resistivity was 15–40 Ω cm and Koolen de-embedding structures were used to determine the parasitic capacitance of the probe pads and to de-embed the short circuit current gain, $|h_{21}|$. Fig. 5 shows a plot of both the embedded and de-embedded $|h_{21}|$ against frequency for an 85 nm L_g device on a 1.8 μm buffer on silicon. The saturation in h_{21} at frequencies <2 GHz is due to gate leakage, and the suppression in the embedded h_{21} at $\sim$1.5 GHz can be eliminated by isolating the device mesa into the Si substrate. Extrapolation of the de-embedded $|h_{21}|$ data from 20 GHz at -20 dB/decade gave a unity gain cutoff frequency, f_T, of 305 GHz at $V_{ds} = 0.5$ V. The RF performance of the InSb QWFET on Si presented here equals that of similar devices previously demonstrated on semi-insulating GaAs substrates [1]. Fig. 6 shows a plot of the intrinsic f_T against DC power dissipation for 85 nm Lg InSb quantum well transistors on both GaAs and silicon substrates and compares these data with those of 60 nm Lg silicon NMOS devices. The InSb QWFETs on both Si and GaAs substrates show more than ten times reduction in DC power dissipation at the same performance compared to the silicon transistors or, equivalently, more than two times increase in intrinsic switching performance at the same power dissipation.

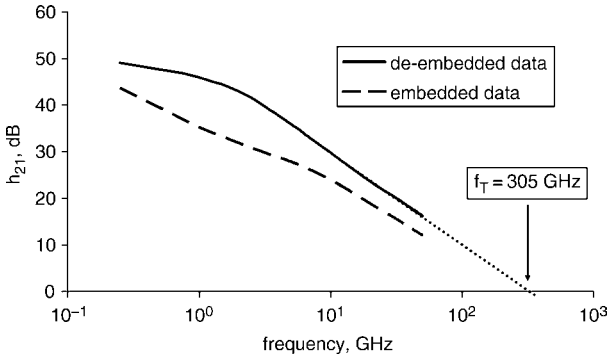

Fig. 5 *Current gain, h_{21}, against frequency for 85 nm Lg InSb QW transistor on 1.8 μm buffer on silicon; $f_T = 305$ GHz, showing raw (embedded) data and de-embedded data*

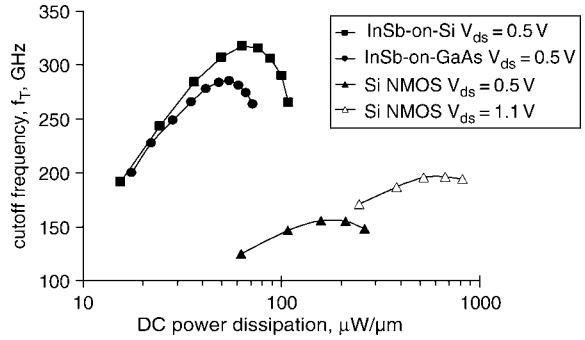

Fig. 6 *De-embedded f_T* against *DC power dissipation for 85 nm Lg InSb QW transistors on silicon or GaAs substrate at $V_{ds} = 0.5$ V, benchmarked against 60 nm Lg silicon NMOS transistors at $V_{ds} = 0.5$ and 1.1 V*

Conclusions: InSb QW material with excellent electrical properties has been demonstrated on (100) Si substrates with a total buffer thickness down to 1.8 μm. Transistors fabricated from this material have intrinsic $f_T = 305$ GHz and saturated transconductance of 710 mS/mm at $V_{ds} = 0.5$ V and thus demonstrate performance characteristics similar to those previously achieved on GaAs. The subthreshold characteristics of InSb QWFETs on Si are compatible with the requirement for future high speed, low power logic. A prerequisite step in demonstrating the feasibility of heterogeneous integration of InSb QW transistors with Si CMOS has been achieved.

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